Amendments to the Claims:

Please cancel claims 41-43 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. - 27. (Canceled)

28. (Previously Presented) A semiconductor device comprising:

a frequency multiplier at an input terminal of the semiconductor device that receives a clock signal having a predetermined frequency, and that generates a first internal clock signal having a frequency that is greater than the predetermined frequency,

a latency controller that controls a latency of the semiconductor device in response to the first internal clock signal and that generates a second internal clock signal according to the latency control result,

a data output buffer that outputs test output data for the semiconductor device in response to the first and second internal clock signals,

wherein the frequency multiplier comprises:

a first pulse signal generating circuit that receives a first clock signal and a second clock signal having the same frequency and that generates a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

a second pulse signal generating circuit that is enabled in response to a first control signal, and that generates a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal, and

an OR circuit that receives the first pulse signal and the second pulse signal, that logically sums the first pulse signal and the second pulse signal, and that outputs the logically summed signal as the first internal clock signal.

29. (Previously Presented) The semiconductor device of claim 28, wherein the first pulse signal generating circuit comprises:

a first differential amplifier that receives the first clock signal and the second clock signal,

and that senses and amplifies a difference between the first clock signal and the second clock signal; and

a first logic circuit that receives an output signal of the first differential amplifier and that generates the first pulse signal in response to the output signal of the first differential amplifier.

30. (Previously Presented) The semiconductor device of claim 28, wherein the second pulse signal generating circuit further comprises:

a second differential amplifier that is enabled in response to the first control signal, and that senses and amplifies a difference between the reference voltage and the first clock signal; and

a second logic circuit that receives an output signal of the second differential amplifier and that generates the second pulse signal in response to the output signal of the second differential amplifier.

31. (Previously Presented) The semiconductor device of claim 28, wherein the data output buffer comprises:

N flip flops, connected in series with each other, that each receive the first internal clock signal, including: a first flip flop that receives data to be output from the semiconductor device and that outputs data in synchronization with the first internal clock signal; and second through Nth flip flops that each receive an output signal of a preceding flip flop in the series and that output the data of the preceding flip flop in synchronization with the first internal clock signal;

an OR circuit that receives output signals of the N flip flops, logically sums the output signals, and outputs the summation signal; and

an output circuit that is synchronized with the second internal clock signal and outputs the summation signal of the OR circuit,

wherein the clock signal frequency of the first internal clock signal is N times greater than the clock signal frequency of the second internal clock signal.

32. (Previously Presented) The semiconductor device of claim 28, wherein the first pulse signal and the second pulse signal have the same pulse width.

33. (Previously Presented) A semiconductor device comprising:

a frequency multiplier at an input terminal of the semiconductor device, that receives a clock signal having a predetermined frequency, and that generates a first internal clock signal having a frequency that is greater than the predetermined frequency,

a latency controller that controls a latency of the semiconductor device in response to the first internal clock signal and that generates a second internal clock signal according to the latency control result, and

a data output buffer that outputs test output data for the semiconductor device in response to the first and second internal clock signals,

wherein the frequency multiplier comprises:

a first pulse signal generating circuit that receives a first clock signal and a second clock signal having the same frequency and that generates a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

a second pulse signal generating circuit that is enabled in response to a first control signal and that generates a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal,

a third pulse signal generating circuit that is enabled in response to a second control signal and that generates a third pulse signal having a third pulse width when a level of the second clock signal is greater than a level of the reference voltage,

a fourth pulse signal generating circuit that is enabled in response to the second control signal, and that generates a fourth pulse signal having a fourth pulse width when a level of the reference voltage is greater than a level of the second clock signal, and

an OR circuit that receives the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal and that outputs the first internal clock signal that is the logical sum of the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal.

34. (Previously Presented) The semiconductor device of claim 33, wherein the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal have the same width.

35. (Previously Presented) The semiconductor device of claim 33, wherein the first control signal is enabled in a dual edge mode and the second control signal is enabled in a quadrature edge mode.

36. (Previously Presented) The semiconductor device of claim 33, wherein the data output buffer comprises:

N flip flops, connected in series with each other, that each receive the first internal clock signal, including: a first flip flop that receives data to be output from the semiconductor device and that outputs data in synchronization with the first internal clock signal; and second through Nth flip flops that each receive an output signal of a preceding flip flop in the series and that output the data of the preceding flip flop in synchronization with the first internal clock signal;

an OR circuit that receives output signals of the N flip flops, logically sums the output signals, and outputs the summation signal; and

an output circuit that is synchronized with the second internal clock signal and outputs the summation signal of the OR circuit,

wherein the clock signal frequency of the first internal clock signal is N times greater than the clock signal frequency of the second internal clock signal.

37. (Previously Presented) The semiconductor device of claim 36, wherein the data output buffer includes 4 flip flops that are connected in series with each other.

38. (Previously Presented) The semiconductor device of claim 33, wherein the first clock signal has a frequency 4 times greater than the second clock signal.

39. (Previously Presented) A method of testing a semiconductor device, the method comprising:

receiving a clock signal having a predetermined frequency and generating a first internal clock signal having greater frequency than the predetermined frequency,

controlling a latency of the semiconductor device in response to the first internal clock

signal and generating a second internal clock signal according to the latency control result, and

outputting test output data for the semiconductor device using the first and second internal clock signals,

wherein generating the first internal clock signal includes:

receiving a first clock signal and a second clock signal and generating a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

generating, in response to a first control signal, a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal, and

logically summing the first pulse signal and the second pulse signal and outputting the signal obtained by the summation as the first internal clock signal.

40. (Previously Presented) A method of testing a semiconductor device, the method comprising:

receiving a clock signal having a predetermined frequency and generating a first internal clock signal having greater frequency than the predetermined frequency,

controlling a latency of the semiconductor device in response to the first internal clock signal and generating a second internal clock signal according to the latency control result, and

outputting test output data for the semiconductor device using the first and second internal clock signals,

wherein generating the first internal clock signal includes:

receiving a first clock signal and a second clock signal having the same frequency and generating a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

generating, in response to a first control signal, a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal,

generating, in response to a second control signal, a third pulse signal having a third pulse width when a level of the second clock signal is greater than a level of the reference voltage,

generating, in response to the second control signal, a fourth pulse signal having a fourth pulse width when a level of the reference voltage is greater than a level of the second clock signal, and

logically summing the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal, and outputting a signal obtained by the summation as the first internal clock signal.

41. - 43. (Canceled)